AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A circuit for monitoring ~~packet information~~ information packets including both data and packet routing information, wherein the information packets are put onto an interconnect by one or more modules, wherein each module has a unique identification on the interconnect and wherein the routing information identifies at least one of the modules associated with the data, said circuit comprising:

circuitry for determining if the information in a packet matches one or more conditions; and

circuitry for preventing a module from putting further information packets onto said interconnect if it is determined that information on the interconnect matches said one or more conditions.

2. (Cancelled)

3. (Original) A circuit as claimed in claim 1, wherein said information comprises requests and responses.

4. (Original) A circuit as claimed in claim 1, wherein said circuitry for preventing a module from putting further information onto the interconnect comprises a register.

5. (Original) A circuit as claimed in claim 4, wherein the register comprises one bit for each module and the value of said bit determines if the respective module is prevented from putting further information into the interconnect.

6. (Original) A circuit as claimed in claim 4, wherein a location is defined in said register for each module, the location being independent of the address of the module used by the interconnect.

7. (Original) A circuit as claimed in claim 1, wherein the module which puts the information onto the interconnect which matches the one or more conditions is prevented by the preventing circuitry from being granted access to the interconnect.

8. (Original) A circuit as claimed in claim 1, wherein the determining circuitry comprises comparator circuitry which compares the information on the interconnect with one or more match conditions.

9. (Currently Amended) A circuit as claimed in claim 1, wherein said conditions comprise one or more preconditions and one or more match conditions, said circuitry for preventing a module from putting information onto said interconnect when said one or more preconditions and said one or more match conditions occur.

10. (Original) A circuit as claimed in claim 9, wherein one precondition is that the one or more match conditions have occurred a predetermined number of times.

11. (Original) A circuit as claimed in claim 9, wherein one precondition is that the circuit is enabled.

12. (Original) A circuit as claimed in claim 9, wherein one precondition is that circuitry external to said circuit has been enabled.

13. (Original) A circuit as claimed in claim 12, wherein said external circuitry is a latch.

14. (Original) A circuit as claimed in claim 9, wherein said match conditions comprise one or more of the following:

an address or address range of the information;

the module or modules which put the information onto the interconnect;

the module or modules which are intended to receive the information on the interconnect; and

the type of transaction to which the information relates.

15. (Original) A circuit as claimed in any preceding claim, wherein storing circuitry is provided to store the information which satisfies the at least one condition.

16. (Currently Amended) A functional circuit comprising: an interconnect;

one or more modules connected to the interconnect; and

a monitoring circuit for monitoring information packets put onto the interconnect by one or more modules, said information packets including both data and packet routing information, wherein each module has a unique identification on the interconnect and wherein the routing information identifies at least one of the modules associated with the data and said monitoring circuit comprising:

circuitry for determining if the information packet on the interconnect matches one or more conditions; and

circuitry for preventing a module from putting further information onto said interconnect if it is determined that information packet on the interconnect matches said one or more conditions.

17. (Original) A circuit as claimed in claim 16, wherein the circuit is an integrated circuit.

18. (Original) A circuit as claimed in claim 16, wherein an arbiter is provided for arbitrating between the modules to determine which module is granted access to the interconnect at a given time, said arbiter being connected to the preventing circuitry, the arbiter and the preventing circuitry being arranged so that a module which is prevented from putting further information onto the interconnect is prevented from winning an arbitration.

19. (Original) A circuit as claimed in claim 18, wherein said determining circuitry is at least partially in the arbiter.

20. (Original) A circuit as claimed in claim 16, wherein said interconnect is a bus.

21. (Original) A circuit as claimed in claim 16, wherein one of said modules comprises a debug module.

22. (Original) A circuit as claimed in claim 16, wherein said preventing circuit is in said debug module.

23. (Original) A circuit as claimed in claim 22, wherein at least part of the determining circuitry is in the debug module.

24. (Currently Amended) A circuit comprising:

an interconnect;

one or more modules connected to the interconnect to put information packets onto the interconnect, wherein the information packets comprise both data and packet routing information, and wherein each module has a unique identification on the interconnect and wherein the routing information identifies at least one of the modules associated with the data;

an arbiter for determining which module is permitted to put information packets onto the interconnect; and

circuitry for preventing a module from putting further information packets onto said interconnect, said preventing circuitry preventing a module from winning an arbitration carried out by said arbiter.

25. (Currently Amended) A method comprising the steps of:

monitoring information packets on an interconnect, the information comprising data and packet routing information and being put onto the interconnect by one or modules, wherein each module has a unique identification on the interconnect and wherein the routing information identifies at least one of the modules associated with the data;

determining if the information on an interconnect satisfies one or more conditions; and

preventing a module from putting information packets onto an interconnect if it is determined that the information satisfies one or more conditions.

26. (Currently Amended) A circuit for monitoring packet information put onto an interconnect by one or more modules, wherein said interconnect is not a

circuit-switched bus, wherein each packet comprises a number of fields containing information, including a routing field, an address field, a source field, a transaction type field, a transaction identifier field, wherein each module has a unique identification on the interconnect and wherein the routing information identifies at least one of the modules, said circuit comprising:

circuitry for determining if the information in a packet matches one or more conditions; and

circuitry for preventing a module from putting further information packets onto said interconnect if it is determined that information on the interconnect matches said one or more conditions.